STUDY MODULE DESCRIPTION FORM

Name of the module/subject		Code
Testing of Digital Systems		**1010802131010812917**
Field of study	Profile of study (general academic, practical)	Year /Semester
Electronics and Telecommunications	**general academic**	**2 / 3**
Elective path/specialty	Subject offered in:	Course (compulsory, elective)
Information and Communication	**English**	**elective**

Cycle of study:	Form of study (full-time,part-time)
Second-cycle studies	**full-time**

No. of hours				No. of credits
Lecture: **2**	Classes: **-**	Laboratory: **1**	Project/seminars: **-**	**3**

Status of the course in the study program (Basic, major, other)	(university-wide, from another field)
major	**from field**

Education areas and fields of science and art	ECTS distribution (number and %)
technical sciences	**3 100%**
Technical sciences	**3 100%**

Responsible for subject / lecturer:

prof. dr hab. inż. Jerzy Tyszer
email: tyszer@et.put.poznan.pl
tel. +48 61 665 3814
Electronics and Telecommunications
ul. Piotrowo 3A 60-965 Poznań

Prerequisites in terms of knowledge, skills and social competencies:

1	**Knowledge**	Knows how to analyze and synthesize digital circuits and systems. Knows basic computer-aided design (CAD) tools used in synthesis and test of digital circuits.
2	**Skills**	Can design a digital circuit taking into account various criteria and by deploying adequate methods and tools. Can use standard libraries, catalog data, application notes, and CAD tools for handling semiconductor circuits and systems.
3	**Social competencies**	Demonstrates responsibility for designed electronic circuits and systems. Is aware of the hazards they pose for individuals and communities if they are improperly designed or produced.

Assumptions and objectives of the course:

This course provides a comprehensive coverage of state-of-the-art digital circuit testing techniques, including practices and automation tools for high-quality low-cost manufacturing test. In addition to fault modeling, test generation and fault simulation, it covers design for testability, built-in self-test for random logic and memory arrays altogether with the newest topics related to embedded test methodologies developed specifically to reduce test data volume, test time, and yield learning.

Study outcomes and reference to the educational results for a field of study

Knowledge:

1. Students acquire a thorough understanding of problems related to fault detection and diagnosis in VLSI combinational and sequential digital circuits, including usage of automated tools for test generation, fault simulation, design for testability, and built-in self-test. - [K2_W12]

2. Students can properly deploy basic fault models, can assess their impact on complexity of both test generation and fault simulation. They are also able to choose an adequate method for test data compression and memory test. - [K2_W12]

3. Students know basics of test economy and relationships between quality of test and reliability of VLSI semiconductor circuits. They can assess the cost of test given a test technology, automated test equipment, timing constraints, and test objectives. - [K2_W12]

Skills:

1. A student can use commercial computer-aided design (CAD) tools to run test pattern generation, fault simulation, scan insertion, and several other tasks related to either testing or designing easy to test digital circuits. - [K2_U15]

2. Using commercial CAD tolls, a student can design a circuit with various test features, including scan chains, test points, on-chip test pattern generators, and test response compactors. - [K2_U15]

3. A student can critically analyze methods proposed to perform fault detection and diagnosis in complex digital designs, including their impact on hardware complexity of test logic, the resultant performance of the circuit and its power budget in the test mode. - [K2_U15]

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Social competencies:

1. Appreciate the practical significance of the VLSI testing and its impact on reliability of digital circuits and systems. - [K2_K05]

Assessment methods of study outcomes

A written final exam is given during the end-of-term exam week. This is followed by considerable discussion among the teaching staff to factor in diligence on the homework and labs, and participation in classes and tutorials. This discussion can affect a final grade for the course.

Course description

This course reviews the most essential and timely issues related to various aspects of testing of microelectronics digital circuits. It is composed of a representative sample of the state of the art solutions in the following areas: economics of test, fault modeling, test pattern generation, fault simulation, design for testability, built-in self-test, fault diagnosis, semiconductor memory test, system-level test, embedded test for high-quality low-cost manufacturing, automation tools and design flows. Special emphasis is placed on issues related to test compression and at-speed testing. All lectures are illustrated with various applications and case studies.

Basic bibliography:

1. M. Abramovici, M.A. Breuer, A.D. Friedman, Digital systems testing and testable design, IEEE Press, New York 1995.
2. L.-T. Wang, C.-W. Wu, X. Wen, VLSI test principles and architectures, Elsevier, Amsterdam 2006
3. H. Jha, S. Gupta, Testing of digital systems, Cambridge University Press, Cambridge 2003.
4. J. Rajski, J. Tyszer, Arithmetic built-in self-test, Prentice Hall, Upper Sadle River 1998.
5. M.L. Bushnell, V.D. Agrawal, Essentials of electronic testing, Kluwer Academic Publishers, Boston 2000.

Additional bibliography:

1. L.-T. Wang, C.-W. Wu, X. Wen, VLSI test principles and architectures, Elsevier, Boston 2006.

Result of average student's workload

Activity	Time (working hours)

Student’s workload

Source of workload	hours	ECTS
Total workload	80	3
Contact hours	50	2
Practical activities	25	1

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